PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Makoto NONAKA

Appln. No.: 09/823,752

Confirmation No.: 9106

Filed: April 03, 2001

For: SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME

Docket No: Q63936

Group Art Unit: 2815

Examiner: George C. ECKERT II

STATEMENT UNDER 37 C.F.R. § 1.97(e)

Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned hereby states, upon information and belief:

That each item of information contained in the Information Disclosure Statement filed concurrently herewith was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of said Information Disclosure Statement.

Respectfully submitted,

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WASHINGTON OFFICE

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PATENT TRADEMARK OFFICE

Date: April 21, 2003

Ref. Q63936

1. The invention related to the following claims of this application is an invention described in the following publications, which had been distributed in Japan or abroad prior to the date of the present application, and therefore, a patent cannot be granted pursuant to Article 29, Section 1, Item 3 of the Japan Patent Law.

2. The invention related to the following claims of this application is based on inventions cited in the following publications, which had been circulated prior to this application in Japan or a foreign country. Because a person having ordinary knowledge in the technical field to which that invention belongs could have easily made the invention prior to this application, a patent cannot be granted pursuant to the stipulations of Article 29, Section 2 of the Japan Patent Law.

Note (For a list of the cited literature, see the List of Cited Literature.)

ORegarding Reason 1

Claims 1 and 2, 7 and 8: Cited Literature 1 through 3

Claims 4 and 5, 11: Cited Literature 1

Claims 9 and 10: Cited Literature 1 and 2

(Remarks)

Claims 1 and 2, 7 and 8: The "semi-custom semiconductor integrated circuit device" described in Cited Literature 1 (refer to paragraphs (0005), (0009) through (0011), and (0016)), the "semiconductor device" described in Cited Literature 2 (refer to paragraphs (0014) through (0027)), and the "semiconductor integrated circuit" described in Cited Literature 3 (refer to paragraphs (0006) through (0014), and (0018)) have the same configuration as the present invention.

Claims 4 and 5, 11: The "semi-custom semiconductor integrated circuit device" described in Cited Literature 1 (refer to paragraphs (0005), (0009) through (0011), and (0016)) has the same configuration as the present invention.

Claims 9 and 10: The "semi-custom semiconductor integrated circuit device" described in Cited Literature 1 (refer to paragraphs (0005), (0009) through (0011), and (0016)) and the "semiconductor device" described in Cited Literature 2 (refer to paragraphs (0014) through (0027)) have the same configuration as the present invention.

ORegarding Reason 2

Claims 1 and 2, 7 and 8: Cited Literature 1 through 3

Claim 3: Cited Literature 1 through 4

Claims 4 and 5, 11: Cited Literature 1

Claim 6: Cited Literature 1, 5

Claims 9 and 10: Cited Literature 1 and 2

(Remarks)

Claims 1 and 2, 7 and 8: Refer to the "semi-custom semiconductor integrated circuit device" described in Cited Literature 1 (refer to paragraphs (0005), (0009) through (0011), and (0016)), the "semiconductor device" described in Cited Literature 2 (refer to paragraphs (0014) through (0027)),

and the "semiconductor integrated circuit" described in Cited Literature 3 (refer to paragraphs (0006) through (0014), and (0018)).

Claim 3: The existence of an input/output buffer arranged below the pad as described in Cited Literature 4 is a well-known technology, and a person skilled in the art could easily conceive of the configuration of the present invention by applying said well-known technology into the devices described in Cited Literature 1 through 3 by means of an arrangement of the input/output buffer—specifically, the input/output element below the pad and the capacitor element.

Claims 4 and 5, 11: Refer to the "semi-customized semiconductor integrated circuit device" described in Cited Literature 1 (refer to paragraphs (0005), (0009) through (0011), and (0016)).

Claim 6: A capacitor element configuration comprising a comb-shaped electrode is a well-known technology as described in Cited Literature 5.

Claims 9 and 10: Refer to the "semi-customized semiconductor integrated circuit device" described in Cited Literature 1 (refer to paragraphs (0005), (0009) through (0011), and (0016)) and the "semiconductor device" described in Cited Literature 2 (refer to paragraphs (0014) through (0027)).

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拒絶理由通知書

特許出願の番号	特願２０００－１００７３２
起案日	平成１５年　２月　５日
特許庁審査官	棚田　一也　　９３６１　４Ｌ００
特許出願人代理人	岩佐　義幸　様
適用条文	第２９条第１項、第２９条第２項

この出願は、次の理由によって拒絶をすべきものである。これについて意見があれば、この通知書の発送の日から６０日以内に意見書を提出して下さい。

理　由

１．この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明であるから、特許法第２９条第１項第３号に該当し、特許を受けることができない。
２．この出願の下記の請求項に係る発明は、その出願前日本国内又は外国において頒布された下記の刊行物に記載された発明に基いて、その出願前にその発明の属する技術の分野における通常の知識を有する者が容易に発明をすることができたものであるから、特許法第２９条第２項の規定により特許を受けることができない。

記　　（引用文献等については引用文献等一覧参照）

○理由１について
請求項１～２，７～８：引用文献Ｎｏ．１～３
請求項４～５，１１：引用文献Ｎｏ．１
請求項９～１０：引用文献Ｎｏ．１～２
（備考）
請求項１～２，７～８；引用文献１（【０００５】，【０００９】～【００１１】，【００１６】段落参照）に記載の「セミカスタム半導体集積回路装置」、引用文献２（【００１４】～【００２７】段落参照）に記載の「半導体装置」、引用文献３（【０００６】～【００１４】，【００１８】段落参照）に記載の「半導体集積回路」は、本発明と同一の構成を有する。
請求項４～５，１１；引用文献１（【０００５】，【０００９】～【００１１】，【００１６】段落参照）に記載の「セミカスタム半導体集積回路装置」は本発明と同一の構成を有する。
請求項９～１０；引用文献１（【０００５】，【０００９】～【００１１】，

【００１６】段落参照）に記載の「セミカスタム半導体集積回路装置」、引用文献２（【００１４】～【００２７】段落参照）に記載の「半導体装置」は、本発明と同一の構成を有する。

○理由２について

請求項１～２，７～８：引用文献Ｎｏ．１～３

請求項３：引用文献Ｎｏ．１～４

請求項４～５，１１：引用文献Ｎｏ．１

請求項６：引用文献Ｎｏ．１，５

請求項９～１０：引用文献Ｎｏ．１～２

（備考）

請求項１～２，７～８；引用文献１（【０００５】，【０００９】～【００１１】，【００１６】段落参照）に記載の「セミカスタム半導体集積回路装置」、引用文献２（【００１４】～【００２７】段落参照）に記載の「半導体装置」、引用文献３（【０００６】～【００１４】，【００１８】段落参照）に記載の「半導体集積回路」を参照されたい。

請求項３；引用文献４に記載されているように、パッド下に入出力バッファを配置することは周知技術であり、引用文献１乃至３に記載のものにおいても該周知技術を採用し、パッドと容量素子の下に入出力バッファすなわち入出力素子を配置し、本発明を構成することは当業者が容易に相当し得たことである。

請求項４～５，１１；引用文献１（【０００５】，【０００９】～【００１１】，【００１６】段落参照）に記載の「セミカスタム半導体集積回路装置」を参照されたい。

請求項６；引用文献５に記載されているように、くし形電極からなる容量素子構造は周知技術である。

請求項９～１０；引用文献１（【０００５】，【０００９】～【００１１】，【００１６】段落参照）に記載の「セミカスタム半導体集積回路装置」、引用文献２（【００１４】～【００２７】段落参照）に記載の「半導体装置」を参照されたい。

引　用　文　献　等　一　覧

１．特開平０９－３０７０６７号公報
２．特開平１０－３１３０９５号公報
３．特開平１１－３０７７２４号公報
４．特開平０１－１０９７４６号公報
５．特開昭６１－２６３２５１号公報

先行技術文献調査結果の記録

・調査した分野　　ＩＰＣ第７版

Ｈ０１Ｌ２１／８２２
Ｈ０１Ｌ２７／０４

この先行技術文献調査結果の記録は、拒絶理由を構成するものではない。